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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/029,649
Filing Date: December 20, 2001
Appellant(s): MCKINNELL, JAMES C.

William J. Breen, III
Reg. No. 45,313
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 07, 2005 appealing from the Office action mailed June 15, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,668,033	Ohara et al.	9-1997
5,702,962	Terasawa	12-1997
6,118,181	Merchant et al.	9-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 4, 6-10, 14-16, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant et al. (U.S. Patent No. 6,118,181), in view of Terasawa (U.S. Patent No. 5,702,962) all of record.

With respect to claim 1, Merchant teaches an electrical device substantially as claimed including:

first (21) and second (23) substrates, having first and second integrated circuits, respectively, wherein at least one of the first substrate or the second substrate has a semiconductor layer (31) thereon; and

a bond structure (33) bonding the first substrate (21) to the second substrate (23), the bond structure (33) including an alloy:

bonded to the semiconductor layer (31);

composed of noble metal (Pd); and

configured to form an electrical connection between the first integrated circuit and the second integrated circuit. (See Fig. 2E, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, *it may be possible to use platinum or other materials for the palladium*. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of using bonded structure composed of noble metal alloyed with an oxide affinity material.

However, Terasawa teaches a bond structure (62) composed of noble metal (Au) alloyed with an oxide affinity material (Sb) to electrically connecting two substrates (10 and 20) together. (See Fig. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to alternatively bond the first and second substrates of Merchant using bonded structure composed of noble metal alloyed with oxide affinity material as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided. (See col. 2, lines 1-24).

With respect to oxide affinity material, Sb is a metal well known to have an affinity for oxygen higher than that of the material (Si) of which the semiconductor layer (10) is composed.

Regarding the term "such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate", note that, there are no native oxide existed between the bond structure and the first and second substrates of Terasawa

'962 and Merchant '181, therefore, the claimed term is met. Furthermore, neither the specification nor the claims define composition of the metal alloy, thus the metal alloy of Terasawa meets the claimed sufficient to remove native oxide.

With respect to claim 3, the electrical device of Merchant further comprising electrical insulation (69) situated between the first (21) and second (23) substrates for electrically isolating a plurality integrated circuits. (See Fig. 2A).

With respect to claim 4, the electrical device of Merchant further comprising a region having a closed environment between the first (21) and second (23) substrates, wherein the region is defined at least in part by the bond structure (33).

With respect to claim 6, the bonding structure bonded to the semiconductor layer (31) of Merchant, in view of Terasawa, is sufficient to maintain an alignment of the first substrate (21) with respect to the second substrate (23).

With respect to claim 7, in view of Terasawa, the alloy (62, Au-Sb) bonded to the semiconductor layer (10) is composed of noble metal (Au) alloyed with an oxide affinity material (Sb), thus, having a free energy that is lower that that of silicon oxide.

With respect to claim 8, in view of Terasawa, the alloy (62, Au-Sb) bonded to the semiconductor layer (10) is composed of noble metal (Au) alloyed with an oxide affinity material (Sb), thus, more probable than not should have a free energy less than a range form about -200 Kcal/mol to about -205 Kcal/mol, as claimed.

With respect to claim 9, the alloy (62) of Terasawa bonded to the semiconductor layer (10) is composed of noble metal alloyed with a material selected from the group consisting of Sb.

With respect to claim **10**, Merchant teaches an electrical device substantially as claimed including: first (23) and second (21) semiconductor wafers including a plurality of integrated circuits, wherein:

the first semiconductor wafer (23) has a silicon layer (31) thereon;

the silicon layer (31) on the first semiconductor wafer (23) is bonded to the second semiconductor wafer (21) by a bonding structure; and

the bonding structure is configured to provide an electrical connection between at least one integrated circuit of the first semiconductor wafer (23) with at least one integrated circuit of the second semiconductor wafer (21). (See Figs. 2E, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of explicitly bonding the wafers using gold alloyed with an oxide affinity material.

However, Terasawa teaches bonding of first (23) and second (21) semiconductor wafers using gold alloyed with an oxide affinity material (Sb). (See Figs. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the semiconductor wafers of Merchant using gold alloyed with an oxide affinity material as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided. (See col. 2, lines 1-24).

With respect to oxide affinity material, Sb is a metal well known to have an affinity for oxygen higher than that of the material (Si) of which the semiconductor layer (10) is composed.

Regarding the term "such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate", note that, there are no native oxide existed between the bond structure and the first and second substrates of Terasawa '962 and Merchant '181, therefore, the claimed term is met. Furthermore, neither the specification nor the claims define composition of the metal alloy, thus the metal alloy of Terasawa meets the claimed sufficient to remove native oxide.

With respect to claim 14, the electrical device of Merchant, in view of Terasawa, further comprising a hermetically sealed region between the first and second semiconductor wafers that is defined in part by:

the silicon layer on the first semiconductor wafer; and

the bonding structure, gold alloyed with the oxide affinity material (Sb).

With respect to claim **15**, Merchant teaches an electrical device substantially as claimed including:

first (23) and second (21) semiconductor wafers each including a plurality of integrated circuits;

silicon (31) on the first semiconductor wafer (23); and

a bonding structure (33) including noble metal, wherein the first semiconductor wafer (23) is bonded to the second semiconductor wafer (21) by the noble metal that is bonded to the silicon (31) on the first semiconductor wafer (23) such that the bonded structure is configured to provide an electrical connection between at least one integrated circuit of the first semiconductor wafer (23) with at least one integrated circuit of the second semiconductor wafer (21). (See Fig. 2B, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of explicitly formed a bond structure including gold alloyed with a material having a free energy lower than that of silicon oxide.

However, Terasawa teaches a bonded structure (62) includes gold alloyed with Sb to provide electrical connection between the first and second semiconductor wafer. (See Figs. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the semiconductor wafers of Merchant by a bonding structure including gold alloyed with Sb as taught by Terasawa because using such material (Au-Sb), the substrates

can be bonded together at lower temperature, thus, warpage can be avoided. (See col. 2, lines 1-24).

With respect to oxide affinity material, Sb is a metal well known to have an affinity for oxygen higher than that of the material (Si) of which the semiconductor layer (10) is composed.

Regarding the term "such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate", note that, there are no native oxide existed between the bond structure and the first and second substrates of Terasawa '962 and Merchant '181, therefore, the claimed term is met. Furthermore, neither the specification nor the claims define composition of the metal alloy, thus the metal alloy of Terasawa meets the claimed sufficient to remove native oxide.

With respect to claim 16, the free energy of the Sb of Terasawa is well known to be less than a range from about -200 Kcal/mol to about -205 Kcal/mol as claimed.

With respect to claim **33**, Merchant teaches an electrical device substantially as claimed including:

first (21) and second (23) substrates bonded together with a first material (33);

the first material having is configured to form an electrical connection between a first integrated circuit on the first substrate (21) with a second integrated circuit on the second substrate (23). (See Fig. 2E, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of using the first material having dispersed therein a reducing agent for the diffusion therein of a second material of which at least one of the first and second substrates is composed.

However, Terasawa teaches a first (10 and second (20) substrates bonded together with a first material (62) having dispersed therein a reducing agent (Sb) for the diffusion therein of oxidation of second material (10) of which at least one of the first (10) and second (20) substrates is composed. (See Fig. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to alternatively bond the first and second substrates of Merchant using the first material having dispersed therein a reducing agent as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided. (See col. 2, lines 1-24).

With respect to the characteristic of the reducing agent, Sb is a metal well known to have an affinity for oxygen higher than that of the Si, thus, Sb is more probable than not should be able to function as reducing agent for the diffusion of oxidation of the second material (Si) as well.

Regarding the term "the first material having the dispersed reducing agent is configured to remove a native oxide and form a electrical contact", since Sb having higher affinity for

oxygen then that of silicon, thus, the metal alloy of Terasawa should be able to remove native oxide (if any existed) on the second material (Si). Also bonding the metal alloy (62) and silicon material (45) of Terasawa forms an electrical connection between the two substrates, therefore, the claimed term is met. Furthermore, neither the specification nor the claims define composition of the metal alloy, thus the metal alloy of Terasawa meets the claimed sufficient to remove native oxide.

With respect to claim 34, in view of Terasawa, the first material (62) comprises gold and the second material (10) comprises silicon.

2. Claims 2, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant '181 and Terasawa '962 as applied to claims 1, 10 and 15 above, and further in view of Ohara et al. (U.S. Patent No. 5,668,033) of record.

With respect to claims 2 and 11, Merchant and Terasawa teaches a bonding structure composed of noble metal, gold, alloyed with an oxide affinity material. It is well known that the lower bonding temperature is determined by the eutectic temperature of the noble metal and silicon.

Thus, Merchant and Terasawa are shown to teach all the features of the claim with the exception of explicitly disclosing the weight of the oxide affinity material in the noble metal alloy.

However, Ohara teaches the noble metal alloy is formed by significantly more Au then oxide affinity material, which is used to break Si-O bond so that good bondage between Au and Si can be achieved. (See col. 6, line 28-col. 9, line 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the bonding structure of Merchant and Terasawa, composed of noble metal alloyed with an oxide affinity material at an amount which is significantly less than the weight of noble metal, less than half, as taught by Ohara to form a bonding structure at lower temperature.

Note that, the higher amount of the oxide affinity material such as Ti, Pt, the higher the temperature of bonding, which lead to warpage.

With respect to claim 17, Merchant and Terasawa teach a bonding structure includes gold alloyed with a material having free energy lower than that of silicon oxide.

Thus, Merchant and Terasawa are shown to teach all the features of the claim with the exception of using the material selected from the group consisting of Ti, Al, Li, Mg and Ca.

However, Ohara teaches: bonding two semiconductor wafers (1 and 22) using a bonding structure including gold alloyed with a material selected from the group consisting of Ti and Al to obtain a good bondage. (col. 8, lines 18-67).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the wafers of Merchant, in view of Terasawa using a boding structure including gold alloyed with a material selected from the group consisting of Ti and Al as taught by Ohara to obtain a good bondage and still be formed at a lower temperature.

(10) Response to Argument

FIRST GROUND OF REJECTION:

Arguments against the references individually:

Against Merchant et al., U.S. Patent No. 6,118,181 (hereinafter Merchant), the Appellant cited Col. 6, lines (sic) 24-23 and 17-19, then concluded: "therefore, Merchant explicitly cautions against the use of materials other than palladium and against the use of eutectic bonding".

The statement appears to that of Appellant's own conclusion rather than that of Merchant's. Merchant, col. 4, lines 20-21, clear teaches: "it should be noted that *other elements* may be used in combination with *or in place of* palladium in layer 27". (emphasis added).

Appellant's argument about the cleanliness of chromium layer 29 surface does not have anything to do with the claimed limitation which called for noble metal alloy with an oxide affinity material on one substrate and silicon on the other substrate.

Appellant adds: nowhere does Merchant disclose, teach or suggest a bond structure having an alloy that is sufficient to remove a native oxide.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Against Terasawa, U.S. Patent No. 5,702,962 (hereinafter Terasawa), Appellant cited various passages indicated that the native oxide are removed by some cleaning processes.

However, the limitations of the claim fail to exclude cleaning of the substrate by any means.

The instant disclosure on the same cleanliness of the wafers, states, ([0024]): when a native oxide is formed upon a surface that is be jointed to another, *it is desirable to remove the native oxide in order to form a strong and uniform bond* to the other surface, and ([0025]): in silicon wafer bonding, where one silicon wafer is bonded to another silicon wafer, *it is desirable to remove native oxide, in any degree of thickness*, from both wafer surfaces that are to form an interface there between. (emphasis added).

Appellant then concludes: "thus, Terasawa disclose the use of acids to remove oxide films and clean surfaces. Nowhere does Terasawa disclose, teach or suggest a bonds structure having an alloy that is sufficient to remove a native oxide".

However, the alloy of Terasawa (Au-Sb) clearly includes an agent (Sb) having an affinity for oxygen higher than that of silicon. Thus, the alloy of Terasawa clearly sufficient to remove a native oxide.

Proposed combination:

The claims are directed to device or apparatus. However, Appellant argues the references in term of a process such as both references teach cleaning prior to bonding of the wafers.

As discussed above, the limitations of the claims do not exclude cleaning of the wafers.

The term "sufficient" is defined by the instant specification as follows ([0031]): "a bond is "sufficient" for the purposes of the present invention when it is capable of maintaining an alignment of wafer 102 with respect to wafer 104 during normal operation of the structure 100.

As such, after the bonding process, the bond should be sufficient to keep wafer 102 attached and aligned to wafer 104 as well being configured to form an electrical connection between the integrated circuit 110 in wafer 102 and the integrated circuits 110 in wafer 104".

The wafers of Merchant, in view of Terasawa are aligned, bonded and electrically connected together during a normal operation, as defined, then the noble metal alloy of Terasawa meets the claimed limitation of sufficient to remove a native oxide from the interface between two wafers.

Product by process limitation:

To simplify the appeal process, the product by process rejection has been removed from the rejection.

Motivation to combine:

Appellant appears to contend that Terasawa runs contrary to the teaching of Merchant.

However, Merchant, col. 3, lines 29-39, clearly suggests that other materials may be used to provide an electrical connection between the two wafers and low temperature is preferred to avoid wafer warpage. The noble metal alloy (Au-Sb) of Terasawa provides exactly that, electronically connection and low temperature.

Therefore, Terasawa is not contrary to but clearly in line with the requirement of Merchant. Thus, the prima facie case of obvious has been established.

Dependent claims:

Since the combination of the Merchant and Terasawa have rendered the independent claims 1, 10, 15 and 33 obvious, as discussed above, the dependent claims 3, 4, 6-9, 14, 16 and 34 are unpatentable over the combination for the same reason discussed above.

SECOND GROUND OF REJECTION:

Appellant repeats the same argument with respect to Merchant and Terasawa and concludes that Ohara does not teach or suggest an alloy that sufficient to remove a native oxide.

Since the noble metal alloy of Terasawa meets the claimed limitation as discussed above. The combination of Merchant, Terasawa and Ohara also render claims 2, 11 and 17 obvious for the same reason discussed above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Anh D. Mai

Conferees:

Mr. David P. Porta, SPE.

Mr. Wael M. Fahmy, SPE.